WHAT IS CLAIMED IS:

1. A clock supply control apparatus which controls supply of a clock signal to first and second devices of a computer system, comprising:

a clock generating unit generating a clock signal;

a clock supply logic unit controlling supply of the clock signal from the clock generating unit to the second device in response to a clock control signal, the second device being operable with the clock signal supplied from the clock supply logic unit; and

a controller setting the clock control signal at one of a clock supply inhibition level and a clock supply allowance level in response to a state of a clock run signal line, the resulting clock control signal being supplied from the controller to the clock supply logic unit,

wherein the first device is operable with the clock signal from the clock generating unit and outputs an interrupt signal to an interrupt signal line regardless of whether the clock control signal is set at the clock supply inhibition level or the clock supply allowance level.

2. A clock supply control apparatus comprising:

a clock generating unit generating a clock signal;

a clock supply logic unit controlling supply of the clock signal from the clock generating unit to a device of a computer system in response to a clock control signal, the device outputting an interrupt signal in response to an operational signal based on the clock signal from the clock supply logic unit; and

a control unit delaying supply of the operational signal to

the device such that the device outputs the interrupt signal in response to the delayed operational signal after the clock signal from the clock supply logic unit is received at the device.

3. The clock supply control apparatus according to claim 2, wherein the device is provided with a card connecter and a card, the operational signal being supplied from the card connector to the device when the card is attached to the card connector, the device outputting the interrupt signal in response to the operational signal.

4. The clock supply control apparatus according to claim 3, wherein the control unit comprises:

a detector detecting whether the card is attached to the card connector; and

a delay unit delaying the supply of the operational signal to the device such that the device outputs the interrupt signal in response to the delayed operational signal after the clock signal from the clock supply logic unit is received at the device.

5. The clock supply control apparatus according to claim 4, wherein the delay unit comprises:

a counter counting the clock signal from the clock supply logic unit; and

a gate circuit outputting the delayed operational signal to the device in response to both an output signal of the counter and an output signal of the detector.

6. The clock supply control apparatus according to claim 4, wherein the delay unit comprises a voltage detection circuit that compares a voltage of an output signal of the detector with a reference voltage internally produced by the detection circuit in order to detect whether the card is attached to the card connector.

7. A clock supply control apparatus comprising:

a clock generating unit generating a clock signal;

a clock supply logic unit controlling supply of the clock signal from the clock generating unit to a device of a computer system in response to a clock control signal, the device being operable with the clock signal supplied from the clock supply logic unit, the device outputting an interrupt signal in response to an operational signal based on the clock signal from the clock supply logic unit; and

a controller setting the clock control signal at one of a clock supply inhibition level and a clock supply allowance level in response to a state of a clock run signal line, the resulting clock control signal being supplied from the controller to the clock supply logic unit,

wherein the controller detects whether the clock signal from the clock supply logic unit is received at the device, and the controller delays supply of the operational signal to the device such that the device outputs the interrupt signal in response to the delayed operational signal after it is detected that the clock signal from the clock supply logic unit is received at the device.

8. A clock supply control method which controls supply of a clock signal to first and second devices of a computer system,

comprising the steps of:

generating a clock signal;

controlling supply of the clock signal from a clock supply logic unit to the second device in response to a clock control signal, the second device being operable with the clock signal supplied from the clock supply logic unit; and

setting the clock control signal at one of a supply inhibition level and a supply allowance level in response to a state of a clock run signal line, the resulting clock control signal being supplied to the clock supply logic unit,

wherein the first device is operable in accordance with the generated clock signal and outputs an interrupt signal to an interrupt signal line regardless of whether the clock control signal is set at the clock supply inhibition level or the clock supply allowance level.

9. A clock supply control method comprising the steps of:

generating a clock signal;

controlling supply of the clock signal to a device of a computer system by a clock supply logic unit in response to a clock control signal, the device outputting an interrupt signal in response to an operational signal based on the clock signal from the clock supply logic unit; and

delaying supply of the operational signal to the device such that the device outputs the interrupt signal in response to the delayed operational signal after the clock signal from the clock supply logic unit is received at the device.

10. A clock supply control method comprising the steps of:

generating a clock signal;

controlling supply of the clock signal to a device of a

computer system by a clock supply logic unit in response to a clock control signal, the device being operable with the clock signal supplied from the clock supply logic unit, the device outputting an interrupt signal in response to an operational signal based on the clock signal from the clock supply logic unit;

setting the clock control signal at one of a clock supply inhibition level and a clock supply allowance level in response to a state of a clock run signal line, the resulting clock control signal being supplied to the clock supply logic unit;

detecting whether the clock signal from the clock supply logic unit is received at the device; and

delaying supply of the operational signal to the device such that the device outputs the interrupt signal in response to the delayed operational signal after it is detected that the clock signal from the clock supply logic unit is received at the device.